A Gate Driver for Synchronous Buck Converter with Normally On Semiconductor Switches

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***Abstract*—Synchronous buck converters with normally off MOSFETs are widely used for point of load converters. Recently introduced, normally on, high electron mobility, power devices shown to have excellent switching characteristics with very low on state voltage drop. To drive a normally on MOSFET, a gate drive with bipolar voltage capability is required. Generation of a bipolar voltage from a positive voltage source, requires switched mode power converters leading to reduction in efficiency with an increase in footprint and cost. This paper presents a circuit that will translate the unipolar voltage produced by a standard gate driver to an adjustable bipolar voltage along with bootstrap technique to drive both top and bottom normally on MOSFETs in a synchronous buck converter. A detailed analysis and design of the proposed circuit is presented. Experimental results confirm the operation of the proposed circuit.**

Keywords- Synchronous buck regulator; gate driver; bootstrap; normally on semiconductor

I. Introduction

Wide band gap devices such as SiC JFETs and GaN based high electron mobility transistors (HEMT) have been identified as promising power semiconductor devices due to their excellent switching characteristic along with very low on state voltage drop [1][2]. Normally on SiC based JFETs are commercially available at relatively high voltage rating [1]. A normally on GaN MOSFET has been introduced in [2] with similar voltage rating. One of the difficulty in using these devices in voltage source type power converters is the normally on nature of the power semiconductor device. The switch is on when no gate voltage is applied. Different methods have been developed to provide protection and start up for these type of converters [1][3][4]. A negative voltage is required to turn the device off [5]. If the control circuit has only positive power supply, a switched mode dc/dc converter is required to provide the negative voltage [1]. In, [6][7] a circuit has been developed that translates an uni polar positive voltage pulse to an unipolar negative pulse with the same magnitude. The same circuit has been modified in [8] to make the magnitude of the negative pulse adjustable. For high voltage and relatively high power converters, an additional switched mode power supply used to generate the negative voltage, may not affect the efficiency and footprint of the converter. This paper considers a low power (6W) and low voltage (15V), point of load synchronous buck converter driven by a pair of normally on MOSFETs. A novel voltage translator circuit, that generates an adjustable bipolar gate voltage necessary to drive the normally on switches, from a standard driver producing a positive uni polar voltage waveform has been presented. A bootstrap circuit is used to drive the top MOSFET. A detailed analysis of the proposed circuit along with a step by step design procedure have been given.

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II. Topology

Fig.1 shows the diagarm of the proposed gate driver along with the power circuit of a synchronous buck converter. In this circuit the top and the bottom MOSFETs, M_1 and M_2, are normally on, i.e. at zero gate source voltage the channel is conducting.

V_{DC} is the input voltage, and V_o is the regulated output voltage.

GD is the block diagram of a standard gate driver for a synchronous buck converter implemented with normally off MOSFETs. GD accepts the control signal for the top and the bottom MOSFETs, PWM_1 and PWM_2 with respect to the system ground GND. The PWM is a digital signal with levels $\overline{V}_{CC}$ and ground. The gate driver (GD) for the bottom switch is essentially a voltage level shifter and a current booster circuit. A pulse with an amplitude of $\overline{V}_{CC}$ with respect to the ground, applied at the input PWM_2 of GD is translated to a pulse of an amplitude V_{CC} with respect to the same ground (V_{EE2} is connected to the ground) at the output pin OP_2. Similarly for the top switch, a pulse at the input PWM_1 is translated to a pulse of an amplitude $(V_{CC1} - V_{EE1})$ with respect to the pin V_{EE1} at the output pin OP_1 of GD.

A bootstarp capacitor C_B is used to provide the supply for the top driver, this capacitor is charged through the diode D_B and resistance R_B from the source V_{CC} when the bottom MOSFET is on.

Output of GD, is unipolar. For example at the output pin OP_2, the high level is V_{CC} and the low level is ground or zero. To drive a normally on MOSFET this signal needs to be translated to a bipolar signal, with levels V_P and $-V_N$ respectively with respect to the ground or the V_{EE2}. A circuit with resistance ($R_{1,2}$), capacitance ($C_{1,2}$) and zeners ($Z_{P1,2}$

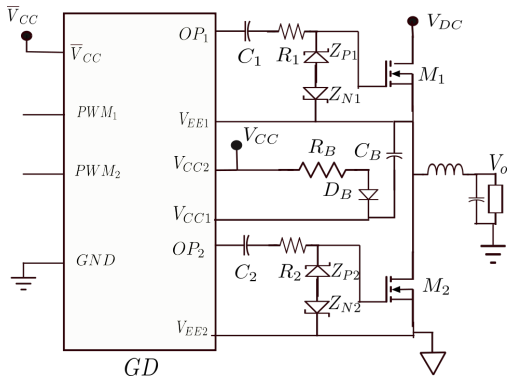

Fig. 1. Proposed gate driver with power circuit of synchronous buck converter.

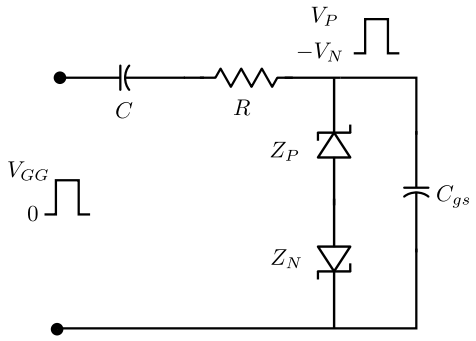

Fig. 2. The voltage translator circuit.

and $Z_{N1,2}$) is used to change the unipolar gate signal to a bipolar one. This circuit is referred as the voltage translator in rest of this paper.

The function of proposed voltage translator circuit is described in the next section.

III. Analysis

Fig.2 shows the diagram of the proposed voltage translator circuit. It translates a voltage pulse with levels V_{GG} and zero to pulse with levels V_P and $-V_N$. The input of this circuit is connected to the output of the gate driver (GD), i.e. OP_2 and V_{EE2} as well as OP_1 and V_{EE1}. The output is connected across the gate and source terminals of the normally on MOSFET. Here, the output load is approximated as the gate source capacitance of the MOSFET, C_{gs} (it can be also modeled as C_{iss} or input capacitance). In this analysis, the forward voltage drop of the zener is neglected. The break down voltage of positive zener, Z_P is V_P, and that of the negative zener Z_N is $-V_N$.

The operation of this circuit is divided into four modes, *MODE I* and *MODE II* are for the transition of the input voltage from zero to V_{GG}, and rest of the two modes correspond to the other transition of the input voltage.

Method of Bootstrapping is used for driving the Top MOSFET M_1. Resistor R_B and diode D_B are used to charge the capacitor C_B via the MOSFET M_2 when it is on.

A. MODE I

Fig.3 shows the equivalent circuit for this mode. At the beginning, the switch was in the off state and the C_{gs} was charged to $-V_N$ and C was charged to V_N. Equations governing this mode are given as (1) and (2).

$$V_{GG} = v_C(t) + Ri(t) + v_{gs}(t) \tag{1}$$

$$i(t) = C\frac{dv_C}{dt} = C_{gs}\frac{dv_{gs}}{dt} \tag{2}$$

Solving (1) and (2), we get (3) and (4) showing how the gate source voltage, $v_{gs}(t)$ and capacitor voltage, $v_C(t)$ change with time, where $\tau = \dfrac{RCC_{gs}}{C + C_{gs}}$.

$$v_{gs}(t) = -V_N + V_{GG}\frac{C}{C + C_{gs}}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{3}$$

$$v_C(t) = V_N + V_{GG}\frac{C_{gs}}{C + C_{gs}}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{4}$$

The gate drive current, *i(t)*, is given in (5).

$$i(t) = \frac{V_{GG}}{R}e^{-\frac{t}{\tau}} \tag{5}$$

For the proper operation of this circuit, the gate source voltage should reach V_P before reaching its final or steady state value $\left(V_{GG}\frac{C}{C+C_{gs}} - V_N\right)$. This leads to the condition (6).

$$C \geq \frac{C_{gs}}{\frac{V_{GG}}{V_P+V_N} - 1} \tag{6}$$

The time, t^*, at which the gate source voltage reaches V_P is given by (7). The capacitor voltage and gate driver current at $t = t^*$ is given in (8) and (9).

$$t^* = \tau \ln\left(\frac{1}{1 - \left(\frac{V_N+V_P}{V_{GG}}\right)\left(1 + \frac{C_{gs}}{C}\right)}\right) \tag{7}$$

$$v_C(t^*) = V_N + (V_N + V_P)\frac{C_{gs}}{C} \tag{8}$$

$$i(t^*) = \left(\frac{V_P + V_N}{R}\right)\left(\frac{V_{GG}}{V_P + V_N} - 1 - \frac{C_{gs}}{C}\right) \tag{9}$$

Fig.4 shows the plots of $v_{gs}(t)$, $v_C(t)$ and *i(t)* in this mode. At $t = t^*$, the *MODE I* ends.

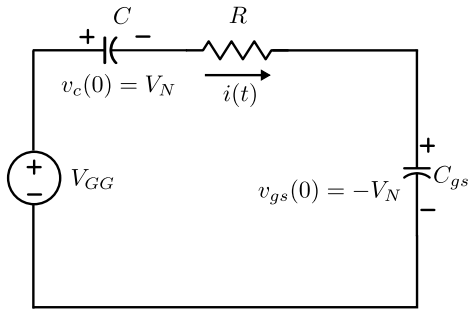

Fig. 3. Equivalent circuit in *MODE I*.

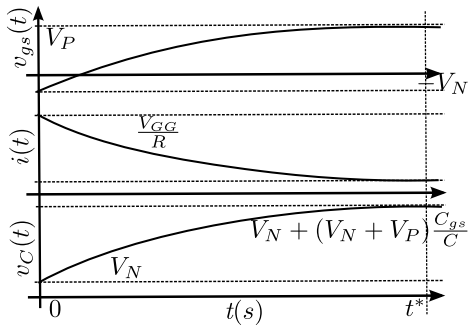

Fig. 4. Plots of $v_{gs}(t)$, $v_C(t)$ and *i(t)* for *MODE I*.

B. MODE II

In *MODE II*, v_C asymptotically reaches $(V_{GG} - V_P)$. The positive zener Z_P breaks down at V_P and maintains a constant voltage of V_P across the gate source terminals of the MOSFET. Fig.5 shows the equivalent circuit for this mode. The gate source terminal has been modeled as constant voltage source V_P.

The equations governing this mode are given in (10) and (11).

$$V_{GG} = Ri(t) + V_P + v_C(t) \tag{10}$$

$$i(t) = C\frac{dv_C}{dt} \tag{11}$$

Solving (10) and (11), we get the equations describing gate drive current and capacitor voltage as (12) and (13).

$$i(t) = \left(\frac{V_{GG} - v_C(0) - V_P}{R}\right) e^{-\frac{t}{RC}} \tag{12}$$

$$v_C(t) = v_C(0) + (V_{GG} - V_P - v_C(0))\, e^{-\frac{t}{RC}} \tag{13}$$

The initial voltage, $v_C(0)$, is given in (8).

Fig.6 shows the plots of $v_{gs}(t)$, $v_c(t)$ and $i(t)$ for this mode.

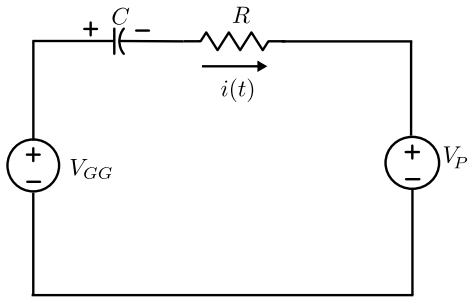

Fig. 5. Equivalent circuit in *MODE II*.

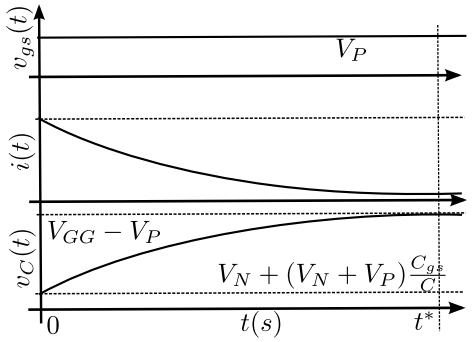

Fig. 6. Plots of $v_{gs}(t)$, $v_C(t)$ and *i(t)* in *MODE II*.

C. MODE III

Fig.7 shows the equivalent circuit for this mode. *MODE III* starts at the transition of gate drive voltage from V_{GG} to 0. Capacitor, C plays a role in driving the gate source voltage in the negative direction upto $-V_N$.

The equations governing this mode are given in (14) and (15).

$$0 = v_C(t) + Ri(t) + v_{gs}(t) \tag{14}$$

$$i(t) = C\frac{dv_C}{dt} = C_{gs}\frac{dv_{gs}}{dt} \tag{15}$$

By solving (14) and (15), we get the equations describing gate source voltage, capacitor voltage and gate drive current as (16), (17) and (18).

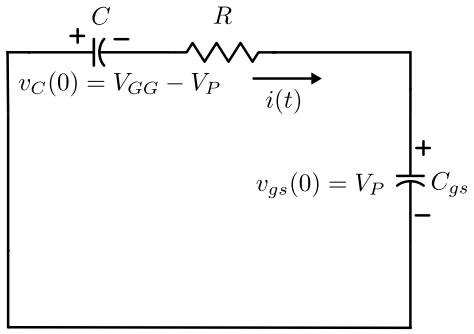

Fig. 7. Equivalent circuit in *MODE III*.

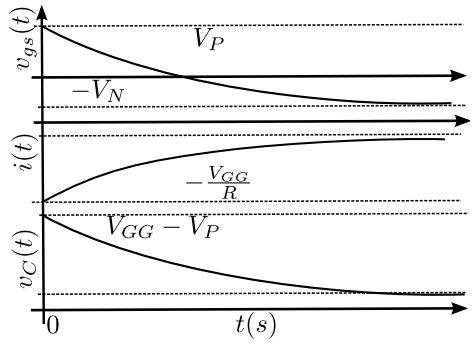

Fig. 8. Plots of $v_{gs}(t)$, $v_C(t)$ and *i(t)* in *MODE III*.

$$v_{gs}(t) = V_P - V_{GG}\frac{C}{C+C_{gs}}\left(1-e^{-\frac{t}{\tau}}\right) \tag{16}$$

$$v_C(t) = V_{GG} - V_P - V_{GG}\frac{C_{gs}}{C+C_{gs}}\left(1-e^{-\frac{t}{\tau}}\right) \tag{17}$$

$$i(t) = -\frac{V_{GG}}{R}e^{-\frac{t}{\tau}} \tag{18}$$

The time taken by gate source voltage to transition from V_P to $-V_N$ is similar in expression as t^* and is given by (7). The capacitor voltage at $t = t^*$ is given in (19).

$$v_C(t^*) = (V_{GG} - V_P) - (V_N + V_P)\frac{C_{gs}}{C} \tag{19}$$

The capacitor, C is responsible for driving the negative voltage across the gate source terminal of the MOSFET. The charge stored in the capacitor is enough to drive the gate source voltage to negative value.

Fig.8 shows the plots of $v_{gs}(t)$, $v_C(t)$ and $i(t)$ for this mode. At $t = t^*$, *MODE III* ends.

D. MODE IV

Fig.9 shows the equivalent circuit in this mode. In *MODE IV*, v_C asymptotically reaches V_N. The negative zener Z_N breaksdown at $-V_N$ and maintains a constant voltage of $-V_N$ across the gate source terminal of the MOSFET.

Equations governing this mode are described in (20) and (21).

$$0 = v_C(t) + Ri(t) - V_N \tag{20}$$

$$i(t) = C\frac{dv_C}{dt} \tag{21}$$

Solving (20) and (21), we get the equations describing capacitor voltage and gate driver current as (22) and (23).

$$v_C(t) = v_C(0) + (V_N - v_C(0))\,(1 - e^{-\frac{t}{RC}}) \tag{22}$$

$$i(t) = \left(\frac{-v_C(0) + V_N}{R}\right)e^{-\frac{t}{RC}} \tag{23}$$

The initial voltage, $v_C(0)$ is given in (19).

Fig.10 shows the $v_{gs}(t)$, $(v_C(t))$ and $i(t)$ for this mode.

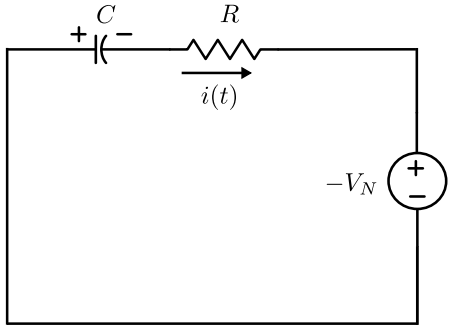

Fig. 9. Equivalent circuit in *MODE IV*.

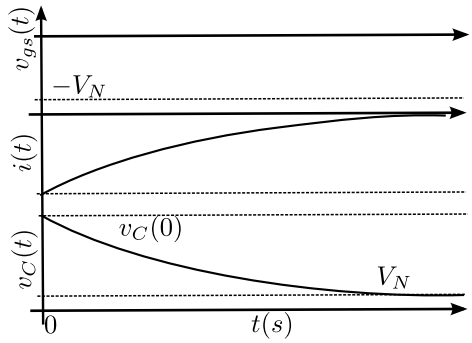

Fig. 10. Plots of $v_{gs}(t)$, $v_C(t)$ and *i(t)* in *MODE IV*.

IV. DESIGN

A synchronous buck converter is designed with the following specification:
Input voltage $V_{DC} = 15V$, output voltage $V_o = 3V$, load current $I_o = 2A$.

The top and bottom MOSFETs are switched at a frequency, $f_s = 250kHz$, in a complementary fashion. The duty cycle of the top MOSFET is 0.2, so the average current through the top and the bottom MOSFETs are $0.4A$ and $1.6A$ respectively. The chosen MOSFET, IXTA6N50D2 has a continuous drain current rating of 6A. From the data sheet $C_{gs} = 2.8\ nF$, but experimentally it has been found to be close to $5.8\ nF$.

Applied gate source voltage decides the on state voltage drop across the drain source terminals of the MOSFET, responsible for conduction loss. From the data sheet of the MOSFET at a gate source voltage of $V_P = 2V$, at a drain current of $2A$, the drain source voltage drop is approximately $0.7V$. The minimum thresh hold voltage is $-4V$. To avoid spurious turn on, the maximum negative gate source voltage when the switch is off is set at $-V_N = -6V$. The gate driver is supplied from the input voltage, so $V_{DC} = V_{CC} = V_{GG} = 15V$. We define a quantity $\lambda = \dfrac{V_{GG}}{V_P + V_N} = 1.875$.

The positive and the negative zeners are chosen with break down voltages at $V_P = 2V$ and $V_N = 6V$. From (24), C must be greater than $\dfrac{C_{gs}}{\lambda - 1}$, let us define $K = \dfrac{C(\lambda-1)}{C_{gs}} > 1$. At the end of *MODE I*, when the positive zener turns on, the entire current that was flowing into C_{gs}, $i(t^*)$, given in (8)

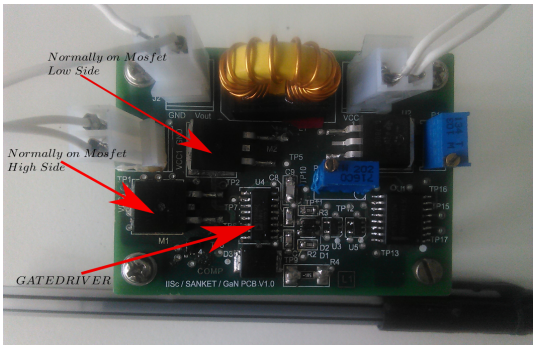

Fig. 11. Top view of the synchronous buck converter circuit

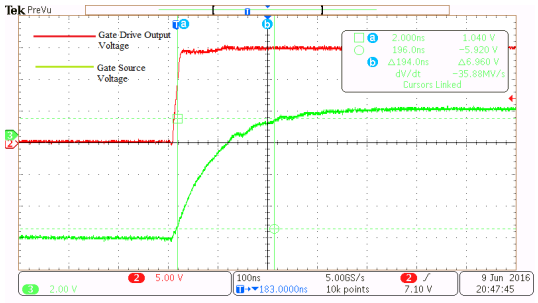

Fig. 12. Gate drive output voltage($V_{OP2} - V_{EE2}$)(5V/div) and gate source voltage (v_{gs})(2V/div) of low side MOSFET(IXTA6N50D2). $t_{rise} = 194\ ns$.

needs to come from the zener. Any inductance in series with the zener will cause an overshoot in the gate source voltage. $i(t^*)$ can be rewritten as (25) with λ and K. According to (25), if we choose K close to 1, this current will be close to zero. We choose $C = 6.8nF$, leading to an effective value of $K = 1.04$. We define rise time t_{rise}, as the time it takes for the gate source voltage to rise from $-V_N + (V_P + V_N)0.1$ to $-V_N + (V_P + V_N)0.9$ in ***MODE I***, similarly t_{fall} time is defined. The resistance R is designed to be 25Ω, such that total of rise and fall time is 10% of the switching period, $\frac{1}{f_s}$ (26).

The gate driver ADuM7234 is selected, so that it can provide a pulse of amplitude $15V$. The peak current capability is $4A > \frac{V_{GG}}{R} = 0.6A$. The power supplied by the driver is $0.115W$, computed using (27). It is less than the rated power of the selected driver.

$$C \geq C_{gs} \frac{1}{\left(\frac{V_{GG}}{V_P + V_N} - 1\right)} = K C_{gs} \frac{1}{(\lambda - 1)} \tag{24}$$

$$i(t^*) = \left(\frac{V_{GG}}{R}\right)\left(1 - \frac{1}{\lambda}\right)\left(1 - \frac{1}{K}\right) \tag{25}$$

$$R = \left(\frac{\lambda + K - 1}{C_{gs} K}\right)\left(\frac{f_s}{0.1}\right)\left(\frac{1 - \ln(\lambda - (0.9(K - 1 + \lambda K)))}{1 - \ln(\lambda - (0.1(K - 1 + \lambda K)))}\right) \tag{26}$$

Power supplied by source is given in (27).

$$P = \lambda K (V_N + V_P)^2 f_s C_{gs} \tag{27}$$

V. Results

Fig.11 shows the top view of the converter. Fig.12 shows the gate driver output voltage and gate source voltage of the low side normally on MOSFET. The rise time is 194 ns, as predicted from the analysis. Fig.13 shows the gate driver output voltage of lower side MOSFET with voltage across gate resistor, indicating gate driver current. These waveforms correspond to *MODE I* and *MODE II*. The circuit is also simulated in MATLAB with the same parameters. Fig.14 provides the same waveforms from simulation. Fig.15

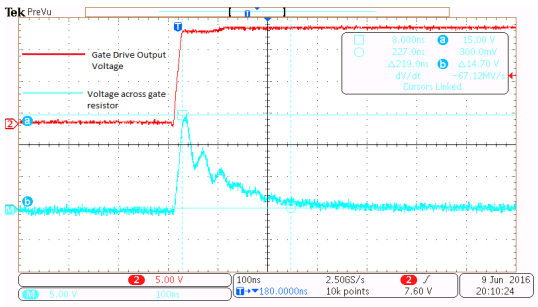

Fig. 13. Gate drive output voltage ($V_{OP2} - V_{EE2}$) and gate resistor voltage (iR) of low side MOSFET(IXTA6N50D2)(5v/div). $(iR)_{peak} = 14.7V$.

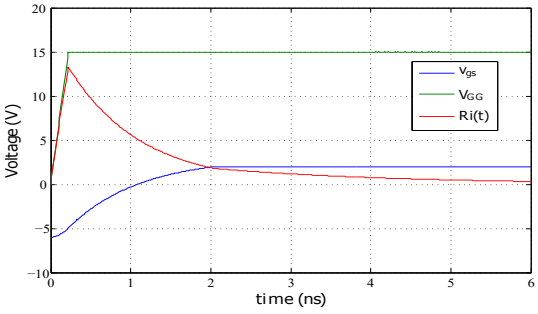

Fig. 14. Simulation results of waveforms obtained by experiment.

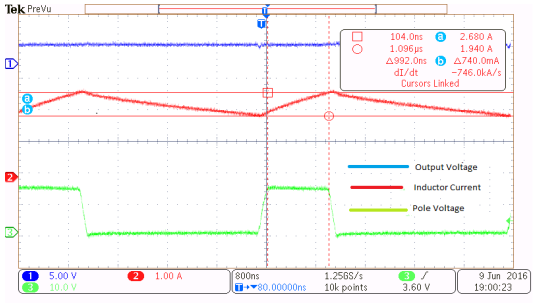

Fig. 15. Output voltage(v_o) (5V/div),inductor current (1A/div),pole voltage (10V/div) of synchronous buck converter. $\delta I_{pk-pk} = 740\ mA$, $t_{on} = 992.0\ ns$.

shows the important voltage and current waveforms of the buck converter operating at $250kHz$ with $15V$ input and $3V$ output supply, with load current of 2A.

VI. Conclusion

In this paper a gate driver circuit with a adjustable bipolar output voltage to drive a normally on MOSFET has been developed. The proposed solution uses a standard unipolar gate driver used for normally off devices in a bootstrap configuration to drive the top and the bottom MOSFETs of synchronous regulator. The proposed circuit does not require any switch mode power supply to generate the negative voltage. A 15V to 3V, 2A synchronous buck converter with normally on MOSFET has been designed, fabricated and tested.

VII. Acknowledgement

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